CH482 Datasheet

V1.6

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2 differential channels 2-to-1, 4-pole 2-throw SuperSpeed analog switch chip CH482D/X

3 differential channels 2-to-1, 6-pole 2-throw SuperSpeed analog switch chip CH483M/X

2 differential channels 4-to-1, 4-pole 4-throw SuperSpeed analog switch chip CH484M

2 differential channels switching, 4-pole 2-throw SuperSpeed analog switch chip CH481D

2 differential channels 4-to-1, 4-pole 4-throw SuperSpeed analog switch chip

CH486F

1. Overview

CH482D, CH483M, CH483X, CH484M, CH481D, CH486F are differential high-speed signal bi-directional analog switch chips based on RF process, high bandwidth and low on-resistance.

CH482D includes 2-channel differential SuperSpeed signal 2-to-1 analog switches with combined QPDT, which can be used for USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G/6G, Display Port and other 2-channel differential signal 2-to-1 switching.

CH482X is similar to CH482D but with higher bandwidth, which can be used for USB 3.1 Gen2 i.e. Super Speed+, PCIe Gen1/2/3, SATA/SAS 3G/6G, Display Port and other 2-channel differential signal 2-to-1 switching.

CH484M includes 2-channel differential SuperSpeed signal 4-to-1 analog switch, combined QPQT, which can be used for USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G, Display Port and other 2-channel differential signal 4-to-1 switching.

CH481D includes 2-channel differential SuperSpeed signal matrix exchange analog switch Exchange Switch, which can be used for USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G/6G, Display Port and other 2-channel differential signal pass-through or crossover. For more multiplexed matrix switching switches or low and medium frequency signal crossover switches, please refer to the CH449 chip manual.

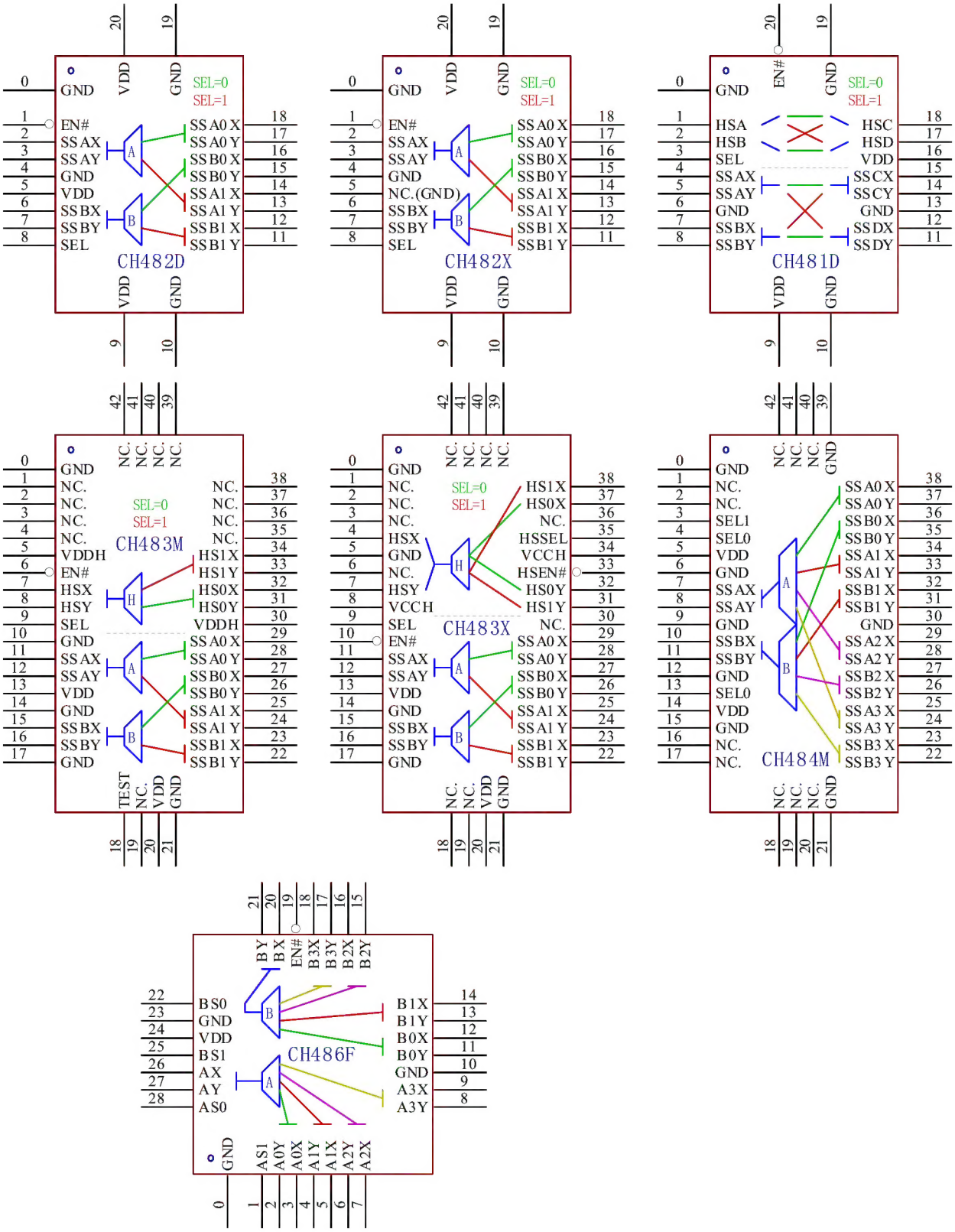
CH486F includes 2-channel differential high-speed signal 4-to-1 analog switches, totaling QPQT, which can be used for 4-to-1 switching of 2-channel differential signals such as USB 2.0 High Speed, SATA/SAS 1.5G, etc. DPOT 8-to-1 switches (8:1 MUX) can be referenced to the CH448 chip.

CH483M and CH483X include all modules of CH482D (referred to as SS Super Speed channel), and also include 1 channel of differential high-speed signal 2-to-1 analog switch (referred to as HS High Speed channel), totaling QPDT+DPDT, which can be used for USB 3.0 Super Speed & USB 2.0 High Speed, PCIe Gen1/2 & Refclk, Display Port and other 3-channel differential signal 2-to-1 switching.

2. Features

- High bandwidth, SS SuperSpeed channel supports 6Gbps differential signals and supports SuperSpeed USB signals.
- CH482X SuperSpeed channel supports 10Gbps differential signaling and supports USB 3.2 Gen2 signaling.
- The HS high-speed channel supports 1.5G(4:1) or 2.5Gbps(2:1) differential signals, and supports full-amplitude voltage analog signals.
- HS high-speed channel supports video signals, low-speed, full-speed and high-speed USB signals.
- Low on-resistance, Ron typical value is about 4Ω.
- Low crosstalk, high isolation.
- Provide global enable pin, multi-channel analog switch unified enable, unified switching.
- SS SuperSpeed channel ESD support 2KV HBM, other channels and control pin ESD support 4KV HBM.
- Support rated 3.3V supply voltage, low static power consumption.
- QFN20-2.5X4.5, QFN42-3.5X9, and QFN28 packages are available and RoHS compatible.

3. Pinouts


CH482D
CH482X
CH481D
CH483M
CH483X
CH484M
CH486F
SEL=0
SEL=1
GND
VDD
EN#
SSAX
SSAY
SSBX
SSBY
SEL
HSA
HSB
HSC
HSD
SSCX
SSCY
SSDX
SSDY
NC.(GND)
NC.
VDDH
HSX
HSY
VCCH
HSSEL
HSEN#
HS1X
HS1Y
HS0X
HS0Y
SEL1
SEL0
SSA0X
SSA0Y
SSB0X
SSB0Y
SSA1X
SSA1Y
SSB1X
SSB1Y
SSA2X
SSA2Y
SSB2X
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SSA3X
SSA3Y
SSB3X
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TEST
BS0
BS1
AX
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AS0
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BY
BX
B3X
B3Y
B2X
B2Y
AS1
A0Y
A0X
A1Y
A1X
A2Y
A2X

Package Form	Body Size	Pin Pitch		Package description	Order Model
QFN20-2.5X4.5	2.5*4.5mmh	0.50mm	19.7mil	Quad Flat No-Lead Package	CH482D
QFN20-2.5X4.5	2.5*4.5mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH482X
QFN42-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH483M
QFN42-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH483X
QFN42C-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH484M
QFN20-2.5X4.5	2.5*4.5mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH481D
QFN28	4*4mm	0.40mm	15.7mil	Quad Flat No-Lead Package	CH486F

Note: QFN packages are labeled with pin 0# on the EPAD, not required but recommended to be connected.

CH483X is for compatible applications only and needs to be pre-ordered; use CH483M or CH482D instead for new designs.

4. Pin Definitions

4.1 CH482D and CH482X Pins

Pin No.	Pin name	Type	Pin description
9/20	VDD	Power	Positive power supply, rated at 3.3V, requires external decoupling capacitor
4/10/19/0	GND	Power	Common ground, digital signal reference ground
5	VDD	Power	CH482D: Optional positive supply, rated 3.3V
	NC.	Reserved	CH482X: No electrical signal connection, it is recommended to connect to GND or VDD
1	EN#	Digital input	Global enable input, low level is effective; high level is disconnected and power is off
8	SEL	Digital input	2-to-1 analog switch selection input: High level selects terminal 1#(SS*1*); Low level selects terminal 0# (SS*0*)
2/3/6/7	SSAX/SSAY/ SSBX/SSBY	Analog signal	Common terminal of the 2-to-1 analog switch
18/17/16/15	SSA0X/SSA0Y/ SSB0X/SSB0Y	Analog signal	The 0# end of the analog switch, the SEL pin input low level selects
14/13/12/11	SSA1X/SSA1Y/ SSB1X/SSB1Y	Analog signal	The 1# end of the analog switch is selected by inputting a high level on the SEL pin.

4.2 CH483M and CH483X Pins

CH483M	CH483X	Pin name	Type	Pin description
13/20	13/20	VDD	Power	Positive power supply for SS SuperSpeed channel, rated at 3.3V
	30	NC.	Reserved	No electrical signal connection, it is recommended to connect to GND or VDD
30/5		VDDH	Power	Positive power supply for HS

				high-speed channel, nominally 3.3V
	8/34	VCCH	Power	Positive power supply for HS high-speed channel, nominally 5V
10/14/17/21/0	5/14/17/21/0	GND	Power	Common ground, digital signal reference ground
18	None	TEST	Analog signal	Reserved. If SS operates at 2.5V supply voltage, it is recommended to short it to VDD to improve performance.
6		EN#	Digital input @VDD domain	Global enable input, active low; high level is disconnected and power is off
	10	EN#	Digital input @VDD domain	SS global enable input, active low; high level is disconnected and powered off
	33	HSEN#	Digital input @VCCH domain	HS global enable input, active low
9	w	SEL	Digital input @VDD domain	Global 2-to-1 analog switch selection input: High level selects 1# terminal (*S*1*); Low level selects 0# terminal (*S*0*)
	9	SEL	Digital input @VDD domain	SS 2-to-1 analog switch selection input: High level selects 1# terminal (SS*1*); Low level selects 0# terminal (SS*0*)
	35	HSSEL	Digital input @VCCH domain	HS 2-to-1 analog switch selection input: High level selects 1# terminal (HS1*); Low level selects 0# terminal (HS0*)
11/12/15/16	11/12/ 15/16	SSAX/SSAY、SSBX/SSBY	Analog signal	Common terminal of SS 2-to-1 analog switch
29/28/27/26	29/28/ 27/26	SSA0X/SSA0Y/ SSB0X/SSB0Y	Analog signal	0# terminal of SS analog switch, SEL pin input low selection

25/24/23/22	25/24/ 23/22	SSA1X/SSA1Y/ SSB1X/SSB1Y	Analog signal	1# terminal of SS analog switch, SEL pin input high selection
7/8	4/7	HSX/HSY	Analog signal	Common terminal of HS 2-to-1 analog switch
32/31	37/32	HS0X/HS0Y	Analog signal	0# terminal of HS analog switch, HSSEL pin input low selection
34/33	38/31	HS1X/HS1Y	Analog signal	1# terminal of HS analog switch, HSSEL pin input high selection
1/2/3/4/19/35/36/37/ 38/39/40/41/42	1/2/3/ 6/18/19/ 36/39/ 40/41/42	NC.	Reserved	No connected, suspended is recommended.

4.3 CH484M Pins

Pin No.	Pin name	Type	Pin description
5/14	VDD	Power	Positive power supply, rated at 3.3V, requires external decoupling capacitor.
6/9/12/15/ 21/30/39/0	GND	Power	Common ground, digital signal reference ground
3	SEL1	Digital input	Selection input SEL1/0 of 4-to-1 analog switch: 00 selects 0# terminal (SS*0*); 01 selects 1# terminal (SS*1*); 10 selects 2# terminal (SS*2*); 11 selects 3# terminal (SS*3*). Pin 4 and pin 13 should be shorted together as SEL0.
4/13	SEL0		
7/8/ 10/11	SSAX/SSAY/ SSBX/SSBY	Analog signal	Common terminal of 4-to-1 analog switch
38/37/ 36/35	SSA0X/SSA0Y/ SSB0X/SSB0Y	Analog signal	0# terminal of analog switch, SEL1/0 pin input 00 is selected.
34/33/ 32/31	SSA1X/SSA1Y/ SSB1X/SSB1Y	Analog signal	1# terminal of analog switch, SEL1/0 pin input 01 is selected.

29/28/ 27/26	SSA2X/SSA2Y/ SSB2X/SSB2Y	Analog signal	2# terminal of analog switch, SEL1/0 pin input 10 is selected.
25/24/ 23/22	SSA3X/SSA3Y/ SSB3X/SSB3Y	Analog signal	3# terminal of analog switch, SEL1/0 pin input 11 is selected.
1/2/16/17/ 18/19/20/ 40/41/42	NC.	Reserved	No electrical signal connection, suspended is recommended.

4.4 CH481D Pins

Pin No.	Pin name	Type	Pin description
9/16	VDD	Power	Positive power supply, rated 3.3V, requires external decoupling capacitor
6/10/13/ 19/0	GND	Power	Common ground, digital signal reference ground
20	EN#	Digital input	Global enable input, active low level; high level is disconnected and powered off
3	SEL	Digital input	Mode input for matrix analog switch: Low level selection pass-through mode (A connects C, B connects D); High level selection switching mode (A connects D, B connects C)
4/5	SSAX/SSAY	Analog signal	SS SuperSpeed channel A port
7/8	SSBX/SSBY	Analog signal	SS SuperSpeed channel B port
15/14	SSCX/SSCY	Analog signal	SS SuperSpeed channel C port
12/11	SSDX/SSDY	Analog signal	SS SuperSpeed channel D port

1	HSA	Analog signal	HS high-speed channel A port
2	HSB	Analog signal	HS high-speed channel B port
18	HSC	Analog signal	HS high-speed channel C port
17	HSD	Analog signal	HS high-speed channel D port

4.5 CH486F Pins

Pin No.	Pin name	Type	Pin description
24	VDD	Power	Positive power supply, rated 3.3V, requires external decoupling capacitor
10/23/0	GND	Power	Common ground, digital signal reference ground
19	EN#	Digital input	Global enable input, active low.
1/28	AS1/AS0	Digital input	Select input of channel A 4-to-1 analog switch: 00 select 0# terminal (A0*); 01 select 1# terminal (A1*); 10 select 2# terminal (A2*); 11 select 3# terminal (A3*)
26/27	AX/AY	Analog signal	Common terminal of channel A 4-to-1 analog switch
3/2	A0X/A0Y	Analog signal	0# terminal of analog switch, AS1/0 pin input 00 is selected.
5/4	A1X/A1Y	Analog signal	1# terminal of analog switch, AS1/0 pin input 01 is selected.
7/6	A2X/A2Y	Analog signal	2# terminal of analog switch, AS1/0 pin input 10 is selected.

9/8	A3X/A3Y	Analog signal	3# terminal of analog switch, AS1/0 pin input 11 is selected.
25/22	BS1/BS0	Digital input	Select input of channel B 4-to-1 analog switch: 00 select 0# terminal (B0*); 01 select 1# terminal (B1*); 10 select 2# terminal (B2*); 11 select 3# terminal (B3*)
20/21	BX/BY	Analog signal	Common terminal of channel B 4-to-1 analog switch
12/11	B0X/B0Y	Analog signal	0# terminal of analog switch, BS1/0 pin input 00 is selected.
14/13	B1X/B1Y	Analog signal	1# terminal of analog switch, BS1/0 pin input 01 is selected.
16/15	B2X/B2Y	Analog signal	2# terminal of analog switch, BS1/0 pin input 10 is selected.
18/17	B3X/B3Y	Analog signal	3# terminal of analog switch, BS1/0 pin input 11 is selected.

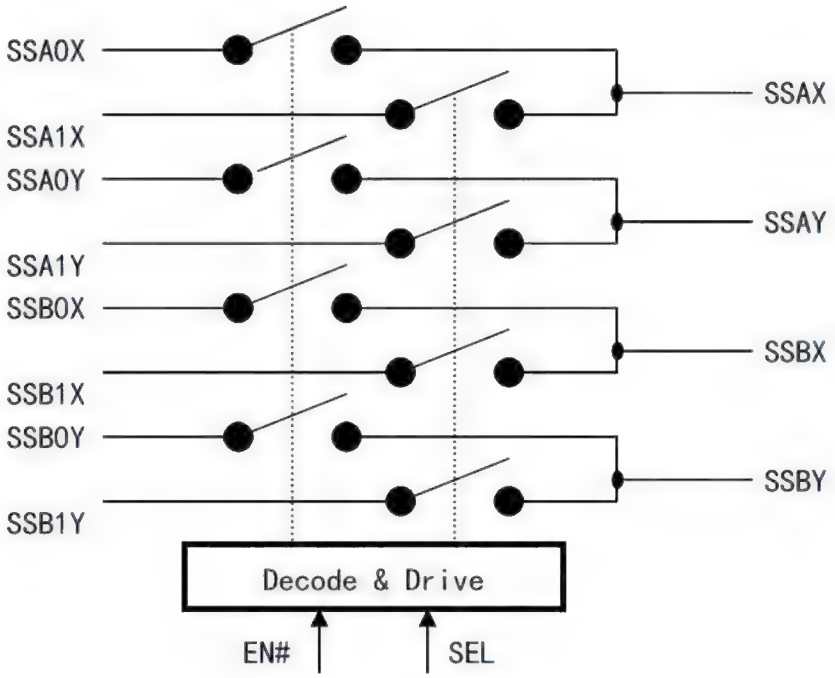
5. Function Description

5.1 CH482D and CH482X

CH482D is a QPDT broadband SuperSpeed bidirectional analog switch chip, which includes 2 differential channel 2:1MUX analog switches (2-to-1 4 channels in total), and can be used for the one-to-one switching of differential signals with voltage not exceeding 1.7V and 6Gbps.

CH482X is a QPDT broadband SuperSpeed d bidirectional analog switch chip, which includes 2 differential channel 2:1 MUX analog switches (2-to-1 4 channels in total). It can be used for the one-to-one switching of differential signals with a voltage not exceeding 1.7V and 10Gbps, and supports USB 3.1/3.2 Gen2.

SSAX and SSAY form a SuperSpeed differential channel SSA; SSBX and SSBY form a SuperSpeed differential channel SSB. Differential signals x and y can be set to +/-(p/n) or vice versa according to the needs of PCB design optimization; Channels SSA and SSB can be set to TX/RX or vice versa according to the needs of PCB design optimization.



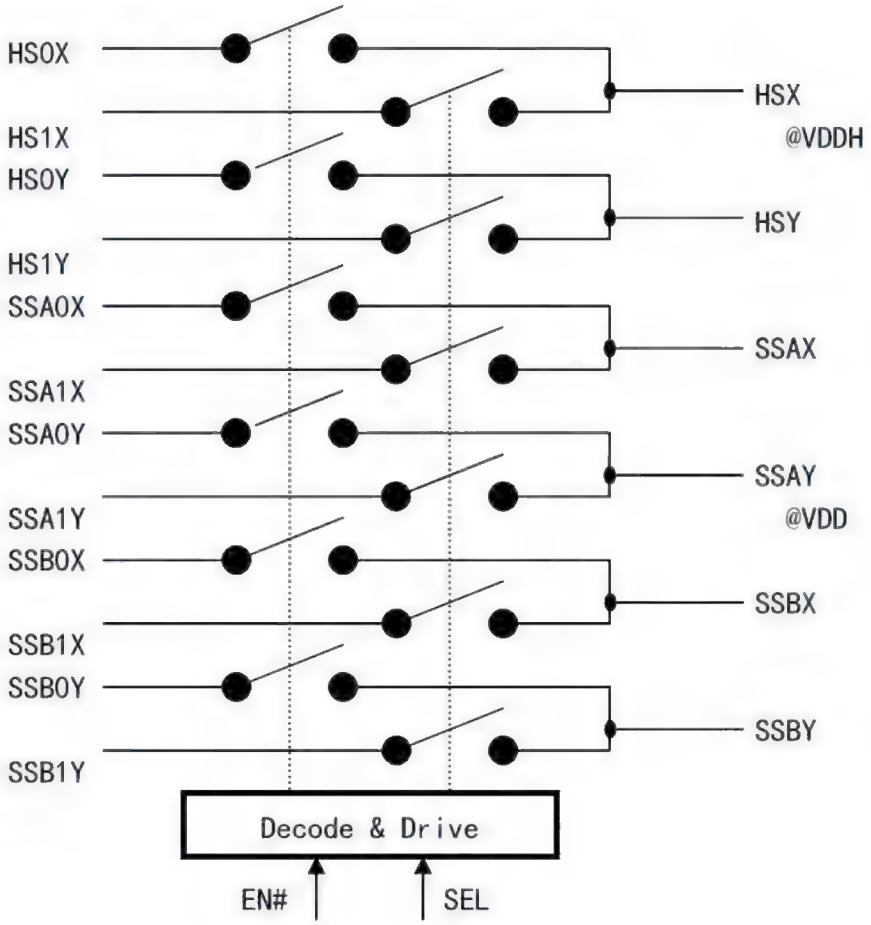
CH482D/X is enabled by EN# pin and switched by SEL pin. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y
1	X	Disconnect all	Disconnect all	Disconnect all	Disconnect all

5.2 CH483M

CH483M is a QDT broadband SuperSpeed bidirectional +DPDT broadband high-speed bidirectional analog switch chip, which includes three differential channel 2:1MUX analog switches (6 channels in total), and can be used to switch the differential signals such as "USB SuperSpeed +USB high speed".

HSX and HSY constitute a high-speed differential channel HS, which supports signals with full VDDH voltage and 2.5Gbps. SS is the same as CH482D chip.



CH483M is uniformly enabled by EN# pin control and uniformly switched by SEL pin selection. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY	HSX	HSY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y	Select HS0X	Select HS0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y	Select HS1X	Select HS1Y
1	X	Disconnect all	Disconnect all	Disconnect all	Disconnect all	Disconnect all	Disconnect all

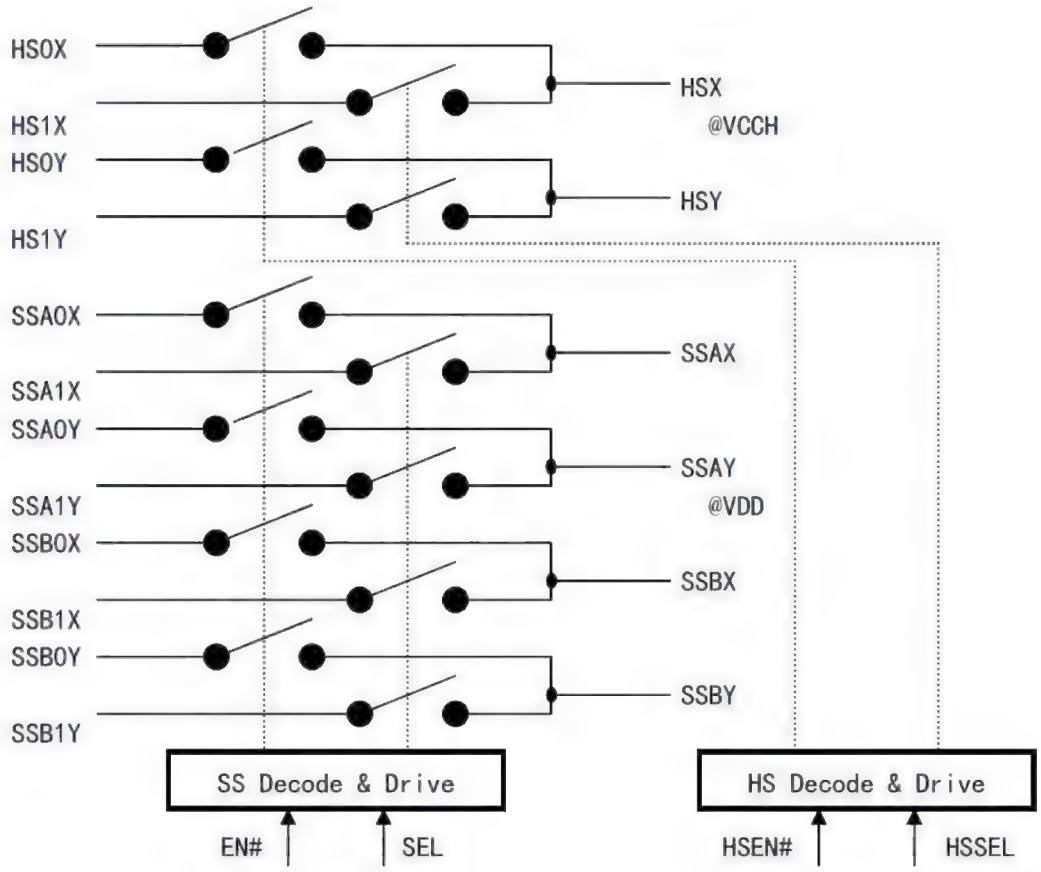
If the SuperSpeed channel SS of CH483M is required to support 2.5V power supply voltage, its TEST pin can be shorted to VDD.

5.3 CH483X

CH483X is a QPDT broadband SuperSpeed bidirectional +DPDT broadband high-speed bidirectional analog switch chip, which includes three differential channel 2:1MUX analog switches (2-to-1 6 channels in total), and can be used for the 2-to-1 switching of differential signals such as "USB SuperSpeed +USB high speed".

HSX and HSY constitute a high-speed differential channel HS, which supports signals with full VCCH voltage and 500Mbps. SS is the same as CH482D chip.

CH483X has 2 main differences compared with CH483M: First, the high-speed channel HS and the SuperSpeed channel SS are completely independent, and each uses independent control signals; Second, the power supply VCCH of the HS channel is rated at 5V. In this case, the HS channel supports 5V full-amplitude signal and the control signal supports 5V or 3.3V.



The SS of CH483X is enabled by EN# pin control and switched by SEL pin selection. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select	Select	Select	Select

		SSA1X	SSA1Y	SSB1X	SSB1Y
1	X	Disconnect all	Disconnect all	Disconnect all	Disconnect all

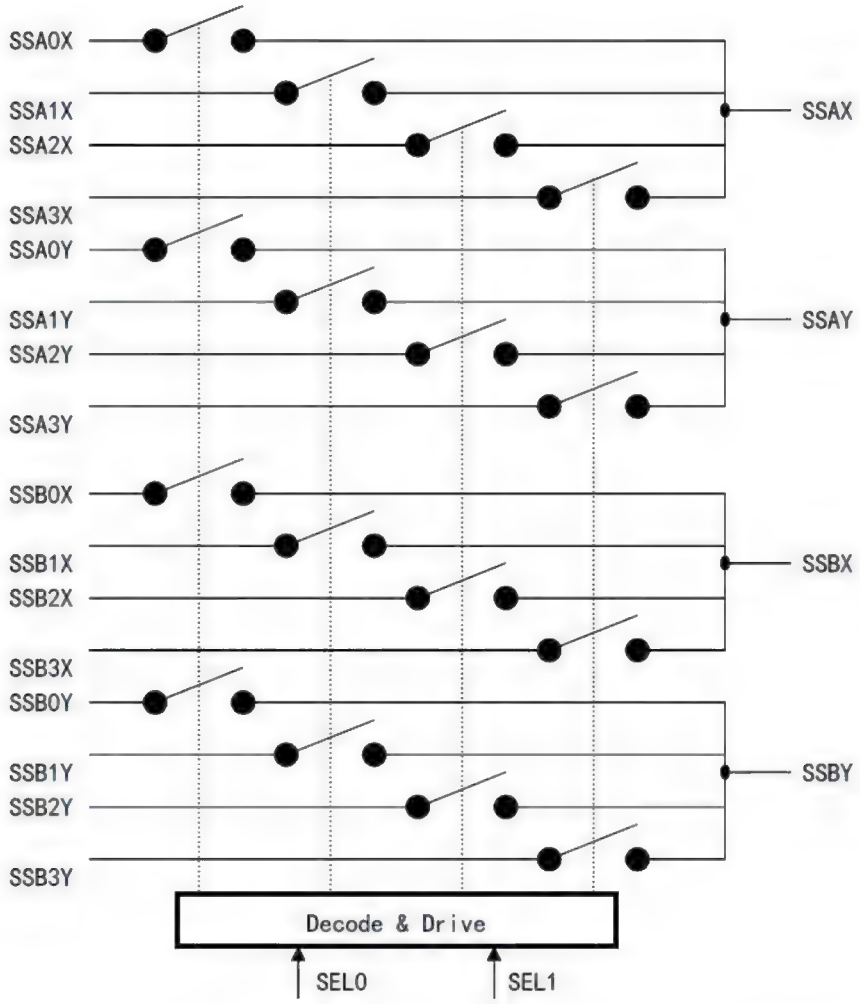
HS of CH483X is enabled by HSEN# pin control and switched by HSSEL pin selection. The following table is its control table.

HSEN#	HSSEL	HSX	HSY
0	0	Select HS0X	Select HS0Y
0	1	Select HS1X	Select HS1Y
1	X	Disconnect all	Disconnect all

5.4 CH484M

CH484M is a QPQT broadband SuperSpeed bidirectional analog switch chip, which includes two differential channel 4:1MUX analog switches (4-to-1 4 channels in total), and can be used for one-of-four switching of differential signals with voltage not exceeding 1.7V and 5Gbps.

SSAX and SSAY form a SuperSpeed differential channel SSA; SSBX and SSBY form a SuperSpeed differential channel SSB. Differential signals x and y can be set to +/-(p/n) or vice versa according to the needs of PCB design optimization; Channels SSA and SSB can be set to TX/RX or vice versa according to the needs of PCB design optimization.



CH484M's channel is always enabled, and the switching of the channel is selected by SEL1 and SEL0 pins. The following table is its control table.

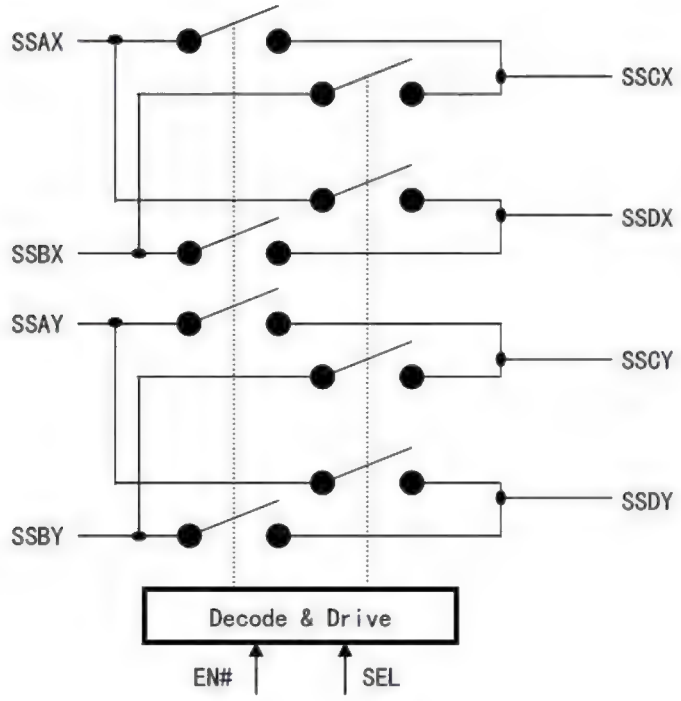
SEL1	SEL0	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y
1	0	Select SSA2X	Select SSA2Y	Select SSB2X	Select SSB2Y

1	1	Select SSA3X	Select SSA3Y	Select SSB3X	Select SSB3Y

5.5 CH481D

CH481D is a 2*2 matrix-switched broadband SuperSpeed analog switch chip, which includes two differential channel 2:2MUX analog switches (2-to-2 2 channels in total Exchange Switch), and can be used for physical layer routing of differential signals with voltage not exceeding 1.7V and 6Gbps.

SSAX and SSAY form SSA port of SuperSpeed differential channel; SSBX and SSBY constitute SSB port of SuperSpeed differential channel, and SSCX and SSCY constitute SSC port of SuperSpeed differential channel; SSDX and SSDY form SSD port of SuperSpeed differential channel. Differential signals X and Y can be set to +/-(p/n) or vice versa according to the needs of PCB design optimization; Ports SSA, SSB, SSC and SSD can be set to TX/RX or vice versa according to the needs of PCB design optimization.



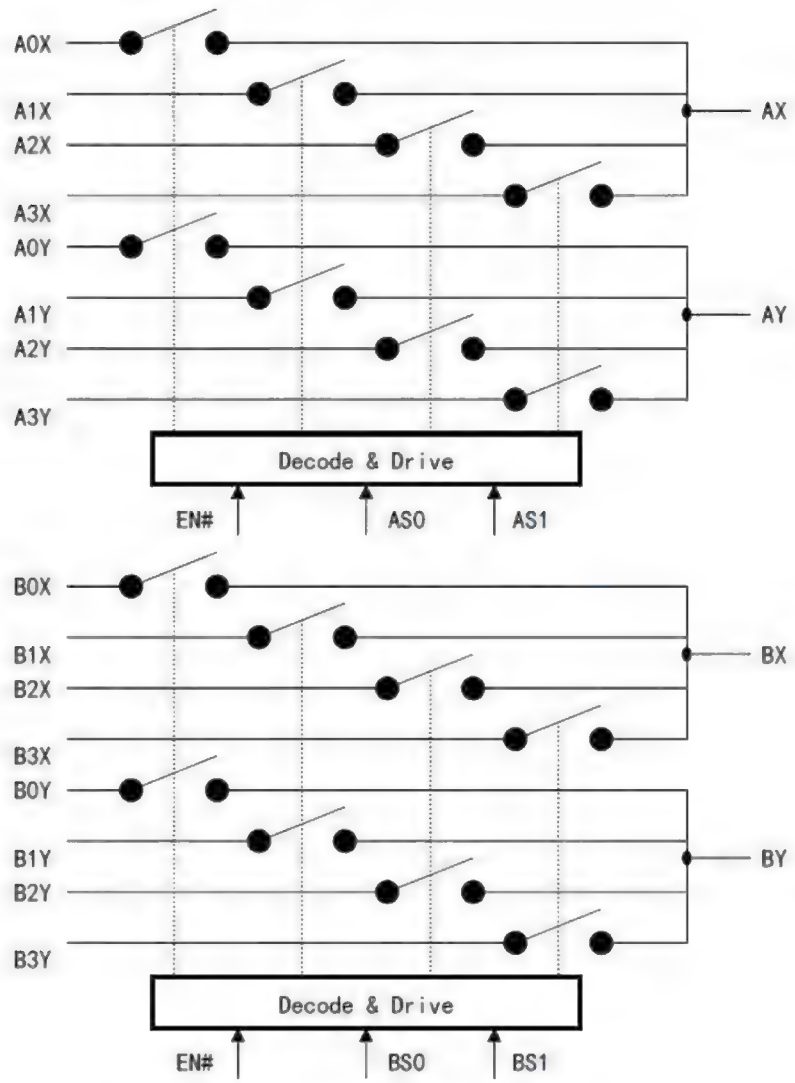
CH481D is uniformly enabled by EN# pin control and switched by SEL pin selection. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY	Description
0	0	Select SSCX	Select SSCY	Select SSDX	Select SSDY	A=C, B=D
0	1	Select SSDX	Select SSDY	Select SSCX	Select SSCY	A=D, B=C
1	X	Disconnect all	Disconnect all	Disconnect all	Disconnect all	

5.6 CH486F

CH486F is a QPQT broadband high-speed bidirectional analog switch chip, which includes two differential channel 4:1MUX analog switches (4-to-1 4 channels in total), and can be used for one-of-four switching of differential signals not exceeding 1.5Gbps.

AX and AY form a high-speed differential channel a; BX and BY form a high-speed differential channel b; The two differential channels are completely independently controlled. Differential signals X and Y can be set to +/-(p/n) or vice versa according to the needs of PCB design optimization; Channels a and b can be set to RX/TX or vice versa according to the needs of PCB design optimization.



CH486F is uniformly enabled by the control of EN# pin, and the switch of channel A is selected by AS1 and AS0 pins, and the switch of channel B is selected by BS1 and BS0 pins. The following table is its control table.

EN#	AS1	AS0	AX	AY
0	0	0	Select A0X	Select A0Y
0	0	1	Select A1X	Select A1Y
0	1	0	Select A2X	Select A2Y

EN#	BS1	BS0	BX	BY
0	0	0	Select B0X	Select B0Y
0	0	1	Select B1X	Select B1Y
0	1	0	Select B2X	Select B2Y

0	1	1	Select A3X	Select A3Y
1	X	X	Disconnect all	Disconnect all

0	1	1	Select B3X	Select B3Y
1	X	X	Disconnect all	Disconnect all

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Symbol	Parameter	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TJ	Operation junction	-40	105	℃
TS	Ambient temperature during storage	-55	150	℃
VCCH	VCCH power supply voltage (VCCH to power, GND to ground)	-0.5	6.0	V
VDD	VDD and VDDH power supply voltage (VDD/VDDH to power, GND to ground)	-0.4	3.8	V
VIOHX	Voltage on CH483X-HS digital or analog input or output pin	-0.4	VCCH+0.4	V
VIOHC	Voltage on digital input pin	-0.3	3.8	V
VIOHS	Voltage on HS analog switch input or output pin	-0.3	VDD+0.3	V
VIOSS	Voltage on SS analog switch input or output pin	-0.3	VDD	V
Isw	Continuous passing current of analog switch	0	10	mA
Iall	Sum of continuous passing currents of all analog switches	0	100	mA

6.2 Thermal Resistance and ESD Characteristics (Test condition: TA = 25℃)

Symbol	Parameter		Min.	Typ.	Max.	Unit
θ_{JA}	Package thermal resistance	QFN20-2.5X4.5		74		℃/W
		QFN42/QFN42C-3.5X9		30		℃/W
		QFN28		57		℃/W
VESD	HBM ESD tolerant voltage	SuperSpeed channel SS	2	3		KV
		CH482X/484M SS channel	1.6	2.5		KV
		HS channel	4	6		KV
		Digital pin	4	6		KV

6.3 CH482/3/4/1 SS Channel Electrical Parameters (Test condition: TA = 25°C, VDD=3.3V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
VDDS	VDD power supply voltage	CH483M (TEST shorted to VDD)	2.5	3.3	3.45	V
		CH482/483X/484/481	3.0	3.3	3.45	V
ICCS	Static supply current, EN#=GND, SEL=VDD or GND			80	800	uA
ICCSD	Power-down supply current，EN#=VDD, SEL=VDD or GND			2	30	uA
VILS	Digital pin low level input voltage		0		0.9	V
VIHS	Digital pin high level input voltage		1.9		VDD	V
ILEAKS	Input leakage current on digital pins			0.2	10	uA
IOFFS	Leakage current of analog switch in the off state @1.7V			±2	±50	uA
VCMS	Recommended voltage range of analog signals		0		1.5	V
VCMXS	Allowable voltage range of analog signal		-0.2		1.7	V
RONS0	Analog switch on resistance, analog signal voltage is 0V			3.5	5	Ω
RONS1	Analog switch on resistance, analog signal voltage is 1.5V			9	13	Ω
RONS0X	CH482X/484M on-resistance, signal voltage is 0V.			5	7	Ω
RONS1X	CH482X/484M on-resistance, signal voltage is 1.5V.			13	17	Ω

6.4 CH483M/6 HS Channel Electrical Parameters (Test condition: TA = 25°C, VDDH=VCCH=VDD=3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDH	High-speed channel HS, CH486 power supply voltage	3.0	3.3	3.45	V
ICCH	Static supply current, HSEN#/HSSEL=VDD or GND，CH486 EN#/SEL/AS/BS=VDD or GND		1	30	uA
ICCXH	Static supply current, *EN#/*SEL/AS/BS=2.3V			500	uA
VILH	Digital pin low input voltage	0		0.9	V
VIHH	Digital pin high input voltage	1.9		VDDH	V
ILEAKH	Input leakage current on digital pins		0.2	10	uA
IOFFH	Leakage current of analog switch in the off state		±0.02	±5	uA
VCMH	Recommended voltage range for analog signals	0		VDDH	V
VCMXH	The voltage range of the allowed analog signal	-0.2		VDDH+0.2	V
RONH0	Analog switch on resistance, analog signal voltage is 0V		3.5	5	Ω
RONH2	Analog switch on resistance, analog signal voltage is 2.5V		9	14	Ω
RONH3	Analog switch on resistance, analog signal voltage is VDDH		7.5	11	Ω

Note: If the analog signal is less than 2.5V, the CH48X chip can also support 2.5V power supply, but the high frequency characteristics are slightly worse and the on-resistance becomes larger.

6.5 CH483X HS Channel 5V Electrical Parameters (Test condition: TA = 25°C, VCCH=5V)

Symbol	Parameter	Min.	Typ.	Max.	Unit

VCCH	Power supply voltage of CH483X high-speed channel HS	4.2	5.0	5.5	V
ICCH5	Static supply current, HSEN#/HSSEL=VDD or GND		0.1	10	uA
ICCXH5	Static supply current, HSEN#/HSSEL=3.4V		1	5	mA
VILH5	Digital pin low level input voltage	0		1.0	V
VIHH5	Digital pin high level input voltage	2.0		VCCH	V
ILEAKH5	Input leakage current on digital pins		0.1	10	uA
IOFFH5	Leakage current of analog switch in the off state		±0.01	±1	uA
VCMH5	Recommended voltage range of analog signals	0		VCCH	V
VCMXH5	Allowable voltage range of analog signal	-0.3		VCCH+0.3	V
RONH50	Analog switch on resistance, analog signal voltage is 0V.		3.7	6	Ω
RONH53	Analog switch on resistance, analog signal voltage is 3.3V		9	14	Ω
RONH55	Analog switch on resistance, analog signal voltage is VCCH.		6	9	Ω

Note: CH483X chip high-speed channel also supports 3.3V power supply, but the on-resistance increases by about 60%. Refer to Section 6.4 for other characteristics.

6.6 CH482/3/4/1 SS Channel Timing Parameters (Test condition: TA = 25℃, VDD=3.3V，VCM=0V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitor, F=1MHz			3	7	pF
DILS	CH482D/CH483 Differential insertion loss	0.1GHz		-0.33		dB
		2.5GHz		-0.6		dB
		4GHz		-1.2		dB
DOIS	Differential off-isolation	0.1GHz		-65		dB
		2.5GHz		-29		dB

		4GHz		-24		dB
DRLS	Differential return loss	0.1GHz		-29		dB
		2.5GHz		-16		dB
		4GHz		-11		dB
NECS	Near end crosstalk	0.1GHz		-70		dB
		2.5GHz		-48		dB
		4GHz		-32		dB
BWS3	CH482D/CH483 analog switch -3dB signal bandwidth		5	7		GHz
BWS2X	CH482X analog switch -3dB signal bandwidth		7	10		GHz
BWS4	CH484M analog switch -3dB signal bandwidth		3	4		GHz
BWS1	CH481D analog switch -3dB signal bandwidth		5	6.5		GHz
TONS	Analog switch on delay, RL=50Ω			1	20	uS
TSWS	Analog switching delay, RL=50Ω			9	80	nS
TOFFS	Analog switch off delay, RL=50Ω			6	25	nS

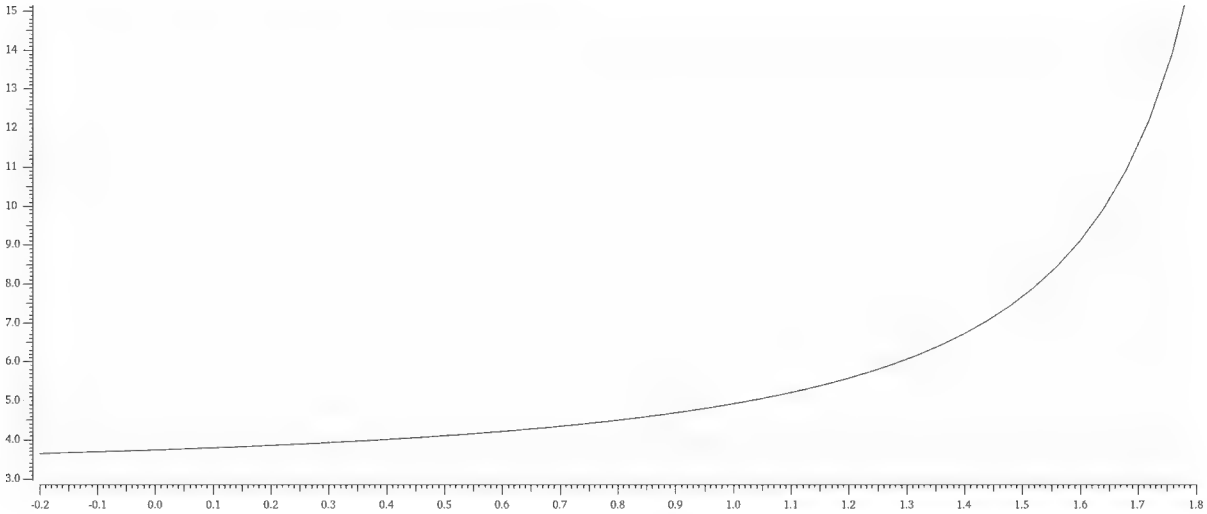
6.7 CH483/6 High-speed Channel Timing Parameters (Test condition: TA=25°C, VDDH/VDD=3.3V, VCM=0V)

Symbol	Parameter			Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance, F=1MHz				3	8	pF
DILH	Differential insertion loss	CH483M-HS	100MHz		-0.3		dB
			1GHz		-1.0		dB
		CH486F	100MHz		-0.32		dB
			1GHz		-1.7		dB
DOIH	Differential off-isolation	CH483M-HS	100MHz		-47		dB
			1GHz		-26		dB
		CH486F	100MHz		-47		dB
			1GHz		-25		dB
DRLH	Differential	CH483M-HS	100MHz		-26		dB

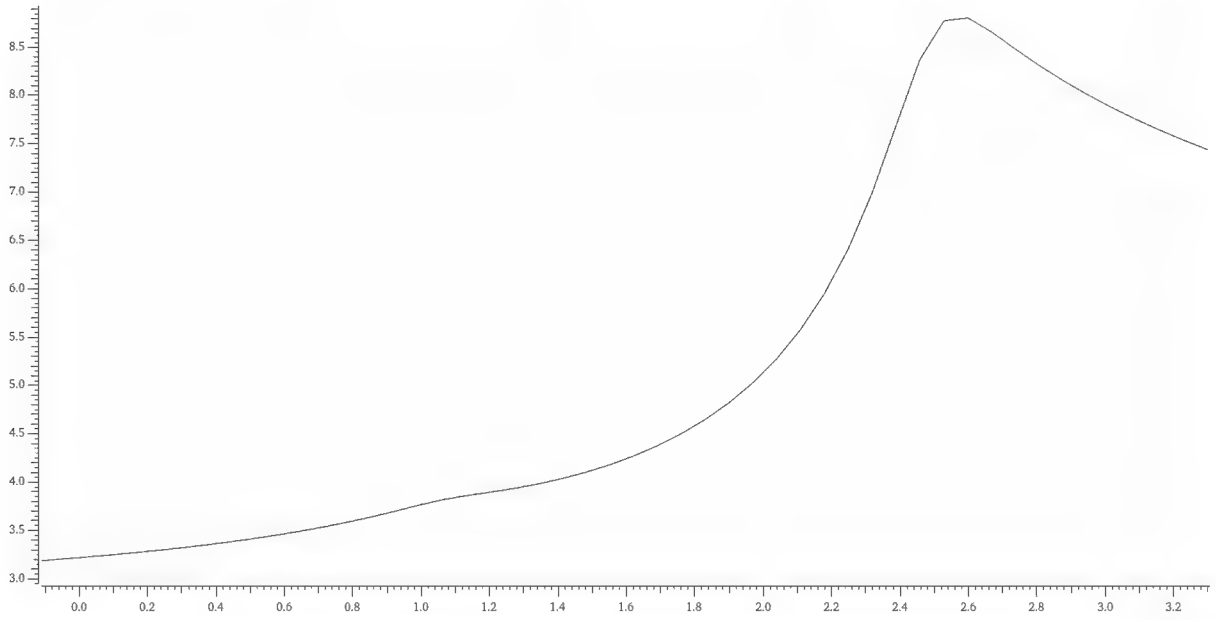
	return loss		1GHz		-9.4		dB
		CH486F	100MHz		-24		dB
			1GHz		-7		dB
NECH	Near end crosstalk	CH483M-HS	100MHz		-84		dB
			1GHz		-35		dB
		CH486F	100MHz		-88		dB
			1GHz		-47		dB
BWH	Analog switch -3dB signal Bandwidth	CH483M-HS		2.0	2.5		GHz
		CH486F		1.3	1.6		GHz
		CH483X-HS		0.35	0.5		GHz
TONH	Analog switch on delay, RL=50Ω				15	40	nS
TSWH	Analog switching delay, RL=50Ω				15	40	nS
TOFFH	Analog switch off delay, RL=50Ω				7	25	nS

6.8 Characteristic Diagram (For reference only. Test conditions: TA = 25°C)

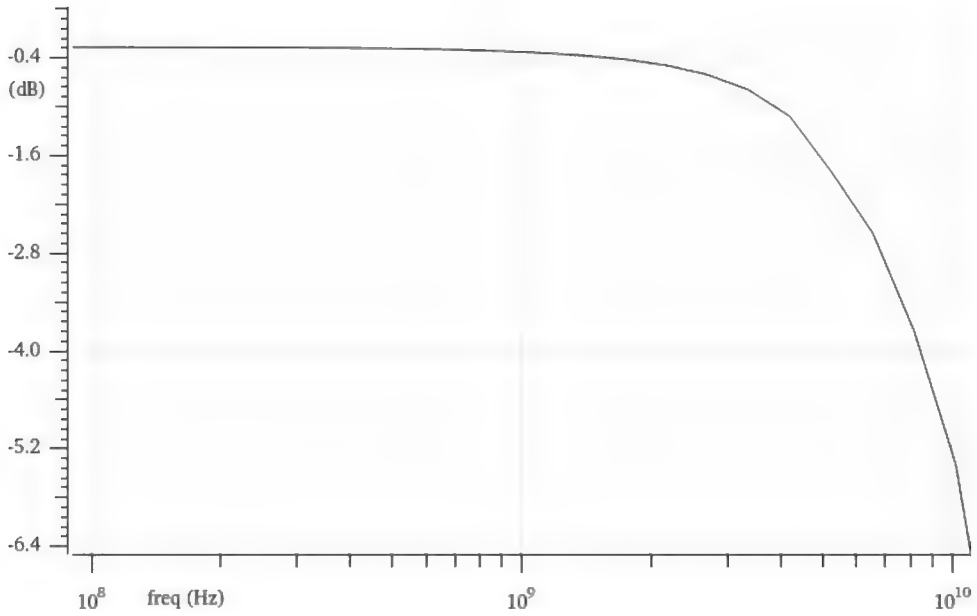
6.8.1 Correlation between on-resistance RON of SS analog switch and analog signal voltage VCOM in CH482D/CH483/CH481D SuperSpeed channel



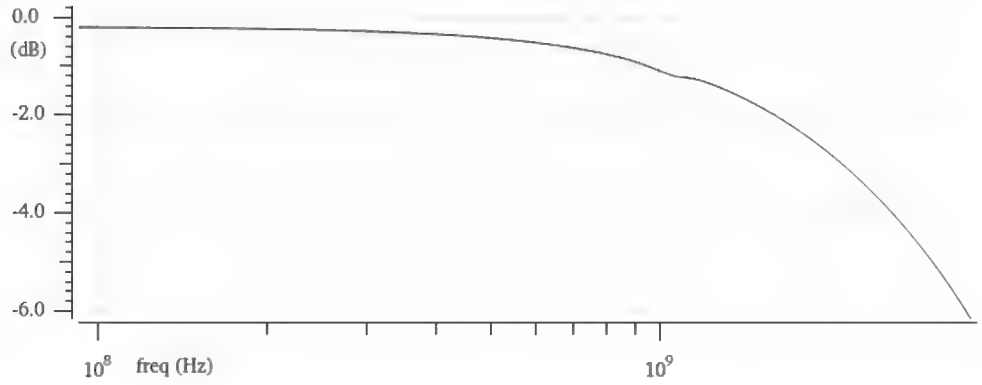
6.8.2 Correlation between on-resistance RON of high-speed channel HS analog switch and analog signal voltage VCOM



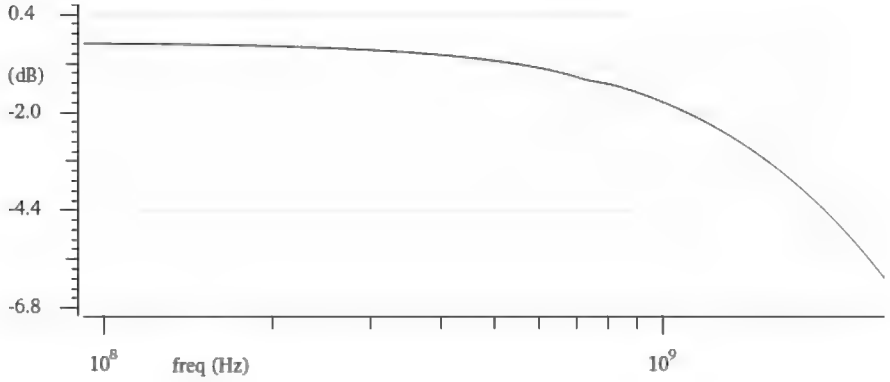
6.8.3 DILS high frequency characteristics of CH482D/CH483/CH481D SuperSpeed channel SS analog switch



6.8.4 DILH high frequency characteristics of CH483M high speed channel HS analog switch



6.8.5 DILS high frequency characteristics of CH482D/CH483/CH481D SuperSpeed channel SS analog switch



7. Applications

7.1 SuperSpeed/High-speed USB Signal Switching

CH48X chips are multiplexer/demultiplexer switches for multi-channel differential signals.

CH483M and CH483X can be used for USB 3.0 SuperSpeed signals and USB 2.0 Hi-Speed signals 2-to-1 synchronous switching.

CH482D can be used for USB 3.0 SuperSpeed signaling with 2-to-1 switching.

CH482X supports 10Gbps signals, but the ESD performance is slightly lower, it is recommended to add an external high-frequency ESD protection device with smaller parasitic capacitance, which can be used for 2-to-1 switching of USB 3.1 and 3.2 Gen2 SuperSpeed+ signals.

The CH484M can be used for USB 3.0 SuperSpeed signaling with 4-to-1 switching.

Analog ports are generally recommended: SSA corresponds to TX, SSB corresponds to RX, X corresponds to + or p, Y corresponds to - or n.

CH486F can be used for 4:1 MUX/DEMUX of USB 2.0 High Speed signal, which has higher bandwidth and better signal compared to CH444.

If used in conjunction with a USB HUB chip such as the CH634, it is recommended that the PCB alignment between the CH48X and the HUB chip be as short as possible and meet the requirements such as impedance matching.

PCB design has a great impact on signal quality, transmission distance, compatibility, etc. It is recommended to refer to the mature design. PCB design must focus on the wiring of high frequency signals (impedance matching, differential pair matching, inter-channel matching, crosstalk and isolation, line width, line spacing, ground plane, EMI, etc.), adjust the optimized pin functions and connections according to the convenience of PCB wiring and additionally place a power supply decoupling capacitor close to the power supply pins. decoupling capacitors near the power supply pins.

7.2 Other Differential or Non-differential Signal Switching

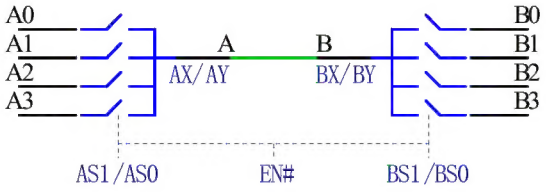
CH482D/X, CH483M/X and CH484M can be used to switch differential signals such as PCIe Gen1/2, SATA/SAS 1.5G/3G and Display Port. CH483M/X also supports synchronous switching of auxiliary differential signal PCIe Refclk.

CH482D/X and CH483M/X can also be used for SATA/SAS 6G and so on, and CH482X can also be used for PCIe Gen3 and so on.

All CH48X chips can be used to switch non-differential signals and video signals.

7.3 CH486F Differential Pairing/Routing

Referring to the following figure, the AX/AY of CH486F is respectively shorted with BX/BY, and the A*X/A*Y port is selected through AS1/0, and the B*X/B*Y port is selected through BS1/0, so that the signal between A* terminal and B* terminal can be re-paired/re-routed. Refer to CH449 for more complex routing.



7.4 Cross/Switch between Signal Pairs

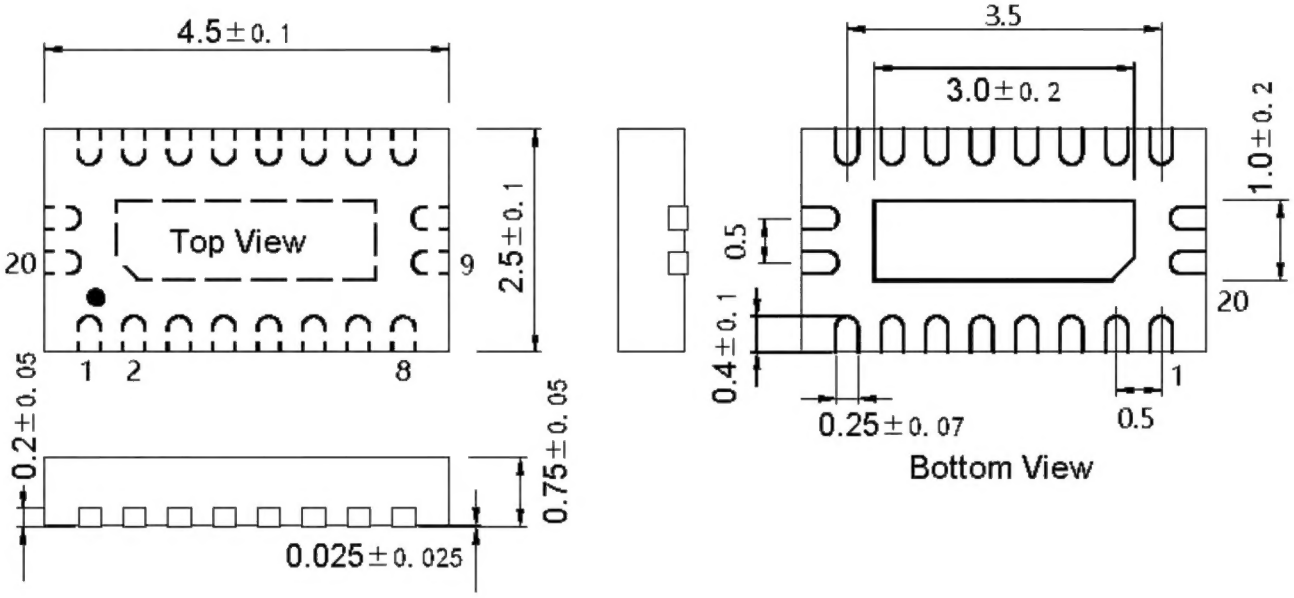
CH481D provides two-in and two-out signal straight-through or switch, which can be used for controllable switch between two differential channels.

8. Package Information

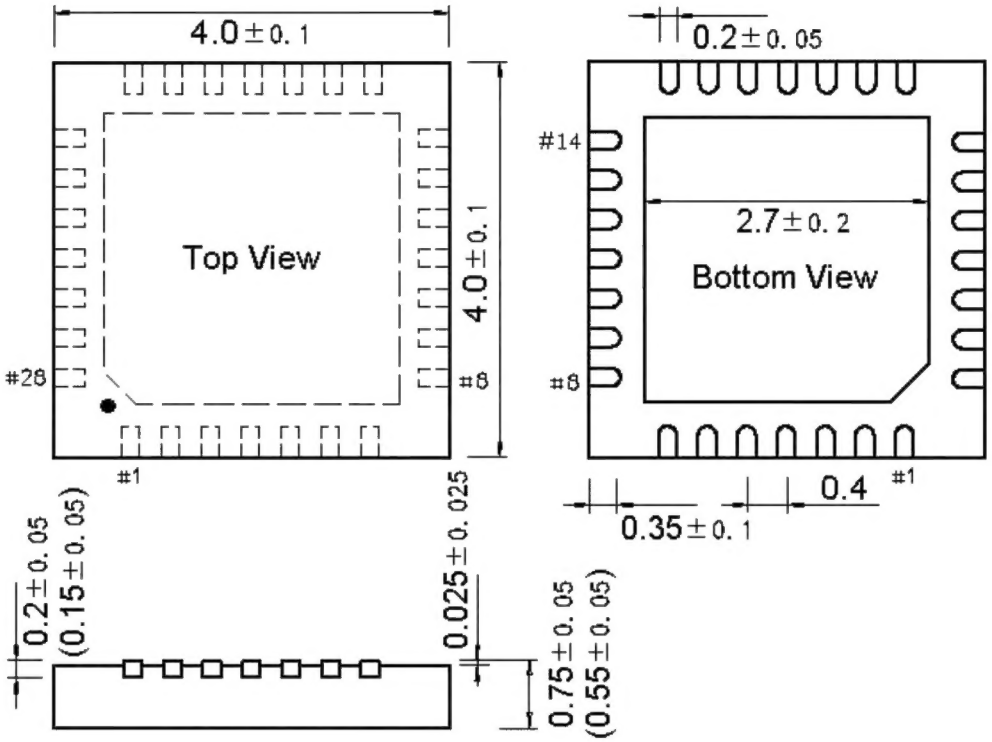
Note: The dimensioning unit is mm.

The pin center distance is a nominal value, no error, and other errors are not more than ±0.2mm.

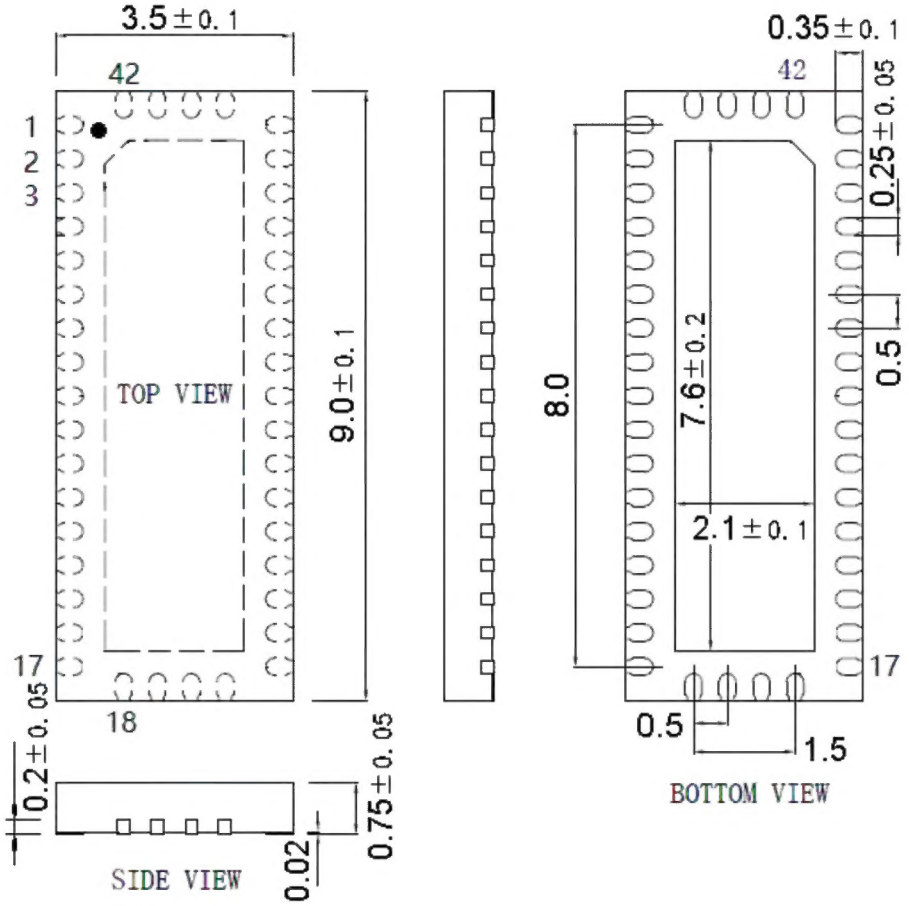
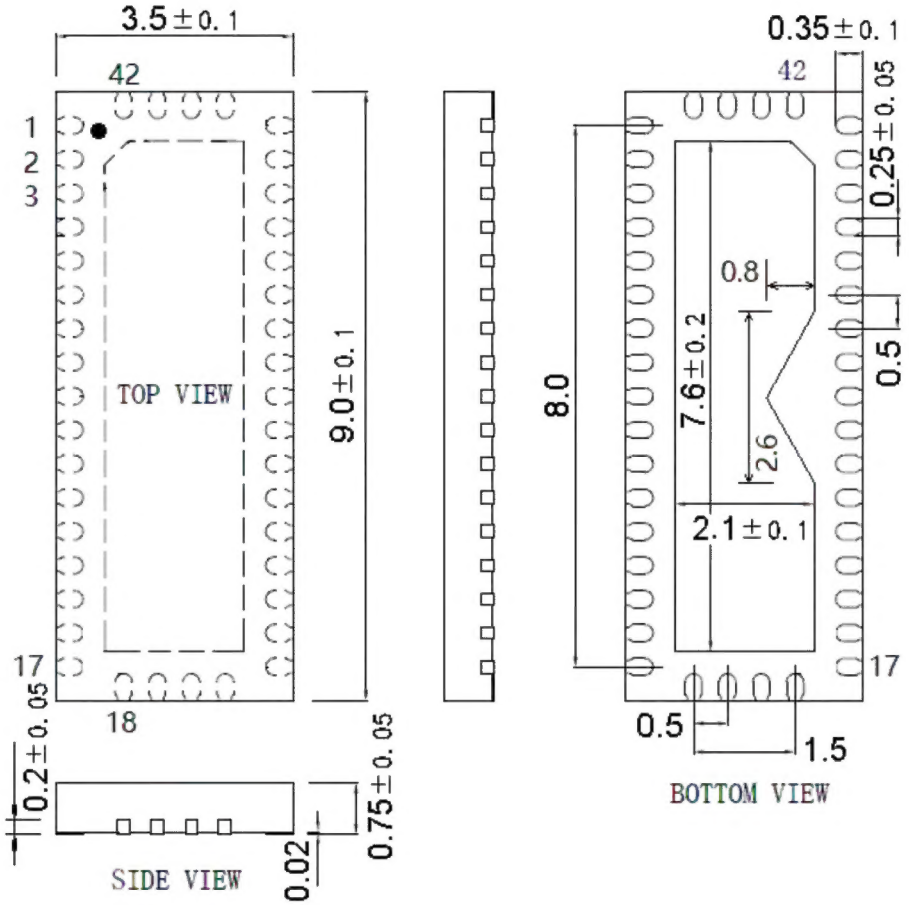
8.1 QFN20-2.5X4.5



8.2 QFN28-4X4



8.3 QFN42-3.5X9 (CH483M/X)



8.4 QFN42C-3.5X9 (CH484M)